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RESEARCH ARTICLE

Design of fault-tolerant reversible Vedic multiplier in quantum cellular automata

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Abstract: In modern computational technologies, a major challenge is the design of devices with smaller size, low power dissipation, and high speed. In order to achieve better optimisation in power dissipation, size and speed, it is necessary to find a technological change. Researchers are trying to find ways and means by introducing many architectural and behavioural changes in the available technologies. One such possible solution is to design digital circuits based on reversible logic and implement them in quantum cellular automata (QCA). In a multiplication process, partial product generation and the addition of partial products are the major factors contributing to the propagation delay. In this paper, Urdhwa Triyakbhyam-based Vedic multiplier using reversible logic is proposed. Vedic multipliers result in faster partial products with less number of steps. Ripple carry adders are used for adding the partial product results to obtain the final product. The multiplier modules are constructed using fault-tolerant reversible KMD gates and hence, the proposed multiplier is a fault-tolerant Vedic multiplier. The designed multiplier is realised in QCA. In the proposed reversible Vedic multiplier, quantum cost is reduced up to 72 %, garbage output is reduced up to 87 %, constant input is reduced up to 87 % and the number of gates are reduced up to 57 % compared to the existing conventional and Vedic multipliers.

Keywords: KMD gates, reversible logic, Urdhwa Triyakbhyam, Vedic multiplication.

INTRODUCTION

In computing, every computing system needs to be optimised in power dissipation, area and speed to be efficient. It is very difficult to achieve all three parameters in a single step with the currently available Complementary Metal Oxide Semiconductor (CMOS) technologies. Moreover, scaling of CMOS limits its performances in many dimensions such as current leakage, noise, interconnections, etc. Hence, it is desirable to move on to other technologies to achieve computational efficiency. Reversible logic-based computation is a better alternative to move towards effective computing systems.

In 1961, Launder invented that losing a bit of information causes heat in the order of kTln2 Joules (where, k - Boltzmann's constant and T - absolute temperature) (Landauer, 1961). This heat is generated due to the bit loss in conventional computation. In 1973, Bennett proposed the reversible logic-based computation, which has a one-to-one unique mapping between the input and output (Bennett, 1973) i.e. the number of inputs and outputs are same. Hence, the kTln2 Joules of heat dissipation is avoided.

Fault detection and avoidance are major problems in digital circuits and it could be achieved by designing a fault-tolerant circuit. Fault-tolerance could be achieved by parity preservation, which means to have an equal parity in inputs and outputs; i.e., exclusive OR gate (XOR) of all the inputs and outputs must be equal (Behrooz, 2006). Therefore, for a reversible logic circuit to be fault-tolerant, it should have parity preservation.

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In a computing system, one of the complicated and time-consuming computations is multiplication. Many researchers have proposed different methods for multiplication in order to speed up the computation of the multiplier. Some of the currently available multipliers are designed with carry-save adder (CSA), carry-select adder and carry-skip adders for fast product generation. Later, special multipliers such as Baugh Wooley multiplier, Wallace multiplier, serial / parallel multiplier and Booth multipliers (Hamacher *et al*., 2011) have been introduced to speed up the process. However, neither the complexity nor the critical path delay in the multiplication process is reduced.

A better alternative solution is Vedic multiplication, which is an ancient way of performing multiplication. Vedic mathematics is reinvented by Sri Bharati Krisna Tirtha from the Indian Veda scriptures. It has 16 sutras and out of them *Nikhilam Sutram*, *Urdhva Tiryakbhayam*, and *Anurupye* are the most popularly used sutras. The advantage of the Vedic multiplier is that it has very simple procedures for complex multiplication (Rakshith *et al*., 2013). The multiplication could be extended to n-bits with some minor modifications.

A n×n reversible Vedic multiplier is proposed and implemented in field-programmable gate array (FPGA) and its resource utilisation is discussed in Poornima *et al*. (2013). A reversible logic-based *Urdhva Tiryakbhyam* multiplication algorithm is implemented in FPGA. Peres, BME and Toffoli gates are utilised to construct the reversible 4×4 Vedic multiplier (Shivarathnamma *et al*., 2016). In Srikanth *et al*. (2014) a 32-bit reversible Vedic multiplier based on *Urdhva Tiryakbhayam* sutra is designed with Peres, HNG and Feynman gate. Here also, Verilog HDL-based design was implemented in FPGA and the delay and power dissipation were analysed.

A 4-bit reversible Vedic multiplication is implemented in FPGA. The multiplier is constructed with Peres, Feynman and NFT gates, in which NFT is a fault-tolerant gate (Rakshith & Saligram, 2013). In this paper, reversible logic performance measures (quantum cost, constant input, garbage outputs) are considered. In Haghparast *et al*. (2009), MKG and HNG reversible gates are introduced for the optimisation in reversible multiplication. The partial product generation is completed with the Peres, HNG gates. More significantly, hardware complexity of the multiplier is measured using logical calculation and a quantum circuit of the gates are introduced.

More recently, a new type of parity preserving gates was analysed (Valinataj, 2017). Here parity preserving gates, double Feynman, Fredkin, NFT, MIG, double Peres and ZPLG (5×5) are discussed. These gates are otherwise named as conservative gates or fault-tolerant gates. A signed multiplier is constructed using these fault-tolerant gates but the multiplier works based on the conventional array multiplication. Thus, its number of gates increases, thereby its hardware complexity is also a little high (Valinataj, 2017).

A detailed procedure to conduct the *Urdhva Tiryagbhyam Sutra*-based Vedic multiplication is explained by (Subramanian *et al*., 2016). An 8-bit multiplier is designed with conventionally available reversible gates such as Peres and Feynman gates. This multiplier acts as a part of the arithmetic logic unit. Further, their performance measures are done using reversible logic parameters (Subramanian *et al*., 2016). The Vedic multiplication costs lower than the booth multiplication.

In Poornima *et al*., (2013), Shivarathnamma *et al*., (2016), Srikanth and Nasam (2016) and Saligram and Rakshith (2013), the final implementation is carried out on FPGA. Since it is a transistor-based approach, low power cosumption and reversibility cannot be assured. The reversible Vedic multiplier were constructed by Rakshith (2013), Haghparast (2009) and Subramanian *et al*. (2016) but they are not fault-tolerant. The fault-tolerant gate was used only by Valinataj (2017), for designing conventional multiplier. Till now, no multiplier was constructed with fault tolerance, reversibility, and realisation in QCA. Hence, the proposed fault-tolerant reversible Vedic multiplier in QCA is very important.

The paper first describes the currently available reversible gates and reviews multipliers. Then it explains the reversible logic metrics and QCA and illustrates the proposed reversible KMD gates and its quantum realisation. Thereafter, the steps of Vedic multiplication process and its QCA realisations are explained. Finally, it compares the conventional multipliers and existing Vedic multipliers with the proposed fault-tolerant reversible Vedic multiplier and concludes the paper stating the usefulness of *Urdhva Tiryakbhayam* multiplier.

METHODOLOGY

Reversible logic metrics and QCA

A reversible gate is expected to have a distinctive mapping between its inputs and outputs; i.e., bijective. It is known as reversibility. In addition, if a reversible gate is capable of generating NOT, AND/NAND & OR/

NOR functions, it is said to be a universal reversible gate (Kalyan, 2014).

The XOR function of inputs and outputs of the reversible gate has to be equal to a fault-tolerant reversible gate [11]. It is otherwise named as parity preservation or conservative logic. Considering I_i's are inputs and O_i's are outputs of a reversible gate, then it should satisfy the following equation (1),

$$I_1 \oplus I_2 \oplus I_3 \ldots \oplus I_n = O_1 \oplus O_2 \oplus O_3 \ldots \oplus O_n \quad \ldots(1)$$

Reversible logic measures slightly deviate from conventional measure metrics. The commonly used reversible logic metrics are quantum cost, garbage output, constant input, and logical calculations.

These metrics are defined as follows,

Quantum cost:
It is the number of 1×1 and 2×2 primitive gates used to realise the desired reversible logic function (Valinataj, 2017).

Garbage output:
The number of outputs not utilised to promote computation is known as garbage output. It is mainly used to maintain the reversibility (Poornima *et al.*, 2013).

Constant input:
It is defined as a stable value (either logical '0' or '1') set in the input of the reversible gate throughout the computation to derive the desired logical output (Poornima *et al*., 2013).

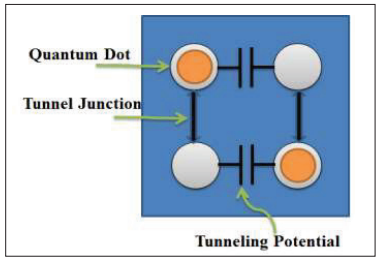
Logical calculation:
It is a measure of the number of XOR (α), AND (β) and NOT (δ) gate functions mandatory to obtain the reversible logic circuit (Haghparast *et al*., 2009).

The realisation of the reversible circuit is performed in quantum cellular automata (QCA). It is a quantum cell consisting of four quantum dots. The position of the electrons defines the logical state of the cell (either logic '0' or '1'). The electrons always occupy diagonally opposite positions as shown in Figure 1 (a, b).

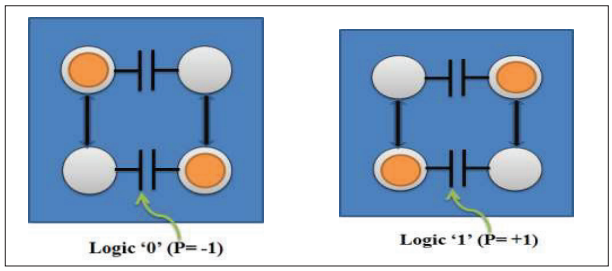
The dimension of the quantum cell is in the order of nanometers. The quantum cellular automata have two major advantages. They are,

i. The computation and information flow (signal propagation) take place simultaneously. It makes the computation and communication faster in QCA.
ii. Each quantum cell is behaving as a computation unit as well as an interconnection line. Therefore, no separate interconnection lines are required.

Because of these two advantages, QCA-based implementation of fault-tolerant reversible logic circuits provides efficiency in power consumption, area, and speed of computation (Sridharan & Pudi, 2015).



(a)



(b)

Figure 1: QCA cell polarised with Logic '0' and Logic '1'

Proposed reversible KMD gates and its QCA realisation

Many researchers are proposing new reversible gates when there is a need to design reversible circuits at an optimum cost. It would be done by either proposing a novel reversible gate or using the combination of available reversible gates configuration. Some of the proposed reversible gates are BME (Shivarathnamma *et al*., 2016), MRG, DKG (Biswas *et al*., 2014), NFT (Rakshith & Saligram, 2013; Ali *et al*., 2015), TSG, MKG, HNG (Haghparast *et al*., 2009), MIG and ZPLG (Valinataj, 2017). These gates mostly satisfy reversibility and universality, but they rarely have the property of fault-tolerance. The characteristics of the proposed and existing reversible gates are shown in Table 1.

In this paper, four fault-tolerant reversible KMD gates are proposed. These gates have reversibility, universality, and fault-tolerance (parity preservation) properties (Kamaraj & Marichamy, 2018). The configuration of KMD gates are depicted in Figure 2 (a, b, c, d).

Table 1: Reversibility, universality and fault tolerance of reversible gates

S. No.	Reversible gate	No. of IOs	Reversibility	Universality	Fault tolerance	Hardware complexity
1.	Feynman	2 × 2	Yes	Yes	No	1α
2.	Fredkin	3 × 3	Yes	Yes	No	2α+4β+1γ
3.	Toffoli	3 × 3	Yes	Yes	No	1α+1β
4.	Peres	3 × 3	Yes	Yes	No	2α+1β
5.	HNG	4 × 4	Yes	Yes	No	5α+2β
6.	MRG	4 × 4	Yes	Yes	No	4α+1β
7.	DKG	4 × 4	Yes	Yes	No	5α+4β+2γ
8.	MKG	4 × 4	Yes	Yes	No	4α+2β+3γ
9.	TSG	4 × 4	Yes	Yes	No	3α+1β
10.	BME	4 × 4	Yes	Yes	No	4α+3β+1γ
11.	MIG	4 × 4	Yes	Yes	Yes	3α+2β+1γ
12.	NFT	3 × 3	Yes	Yes	Yes	3α+3β+2γ
13.	ZPLG	5 × 5	Yes	Yes	Yes	8α+3β+1γ
14.	KMD gate 1	3 × 3	Yes	Yes	Yes	2α+4β+3γ
15.	KMD gate 2	3 × 3	Yes	Yes	Yes	2α+4β+3γ
16.	KMD gate 3	4× 4	Yes	Yes	Yes	5α+3β+1γ
17.	KMD gate 4	5 × 5	Yes	Yes	Yes	6α+4β+2γ

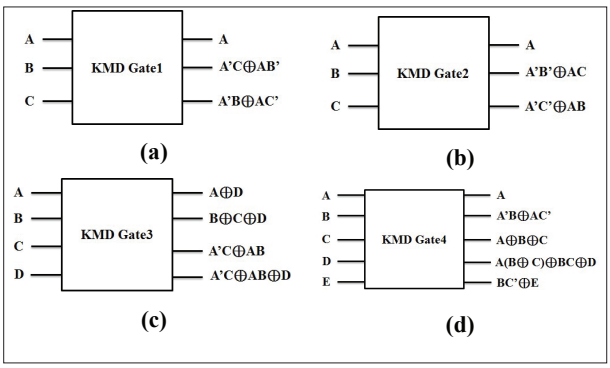


Figure 2: Functional diagram: (a) KMD gate 1; (b) KMD gate 2; (c) KMD gate 3 and (d) KMD gate 4

The KMD gates need a minimum number of cells for its realisation in QCA compared to the previously proposed reversible gates. From Table 2, it is observed that KMD gates require a minimum number of cells for its realisation, and therefore the area occupied gets minimised. The QCA realisation and quantum structure of KMD gates are shown in Figures 3 and 4, respectively.

Vedic multiplier

The literal meaning of *Urdhva Tiryagbhyam Sutra* is 'Vertically and Crosswise'. It performs multiplication in vertical and crosswise and the partial products are

Table 2: Comparison of the cost of the KMD gates

Reversible gates	Number of cells used	Quantum cost	Area (μm^2)
Fredkin gate (Biswas *et al*., 2014)	187	5	0.19
DKG gate (Biswas *et al*., 2014)	752	6	1.24
MRG GATE (Biswas *et al*., 2014)	456	6	0.52
NFT gate (Ali *et al*., 2015)	128	-	0.142
KMD gate 1 (Kamaraj & Marichamy, 2018)	169	10	0.19
KMD gate 2 (Kamaraj & Marichamy, 2018)	121	10	0.13
KMD gate 3 (Kamaraj & Marichamy, 2018)	116	6	0.19
KMD gate 4 (Kamaraj & Marichamy, 2018)	244	12	0.42

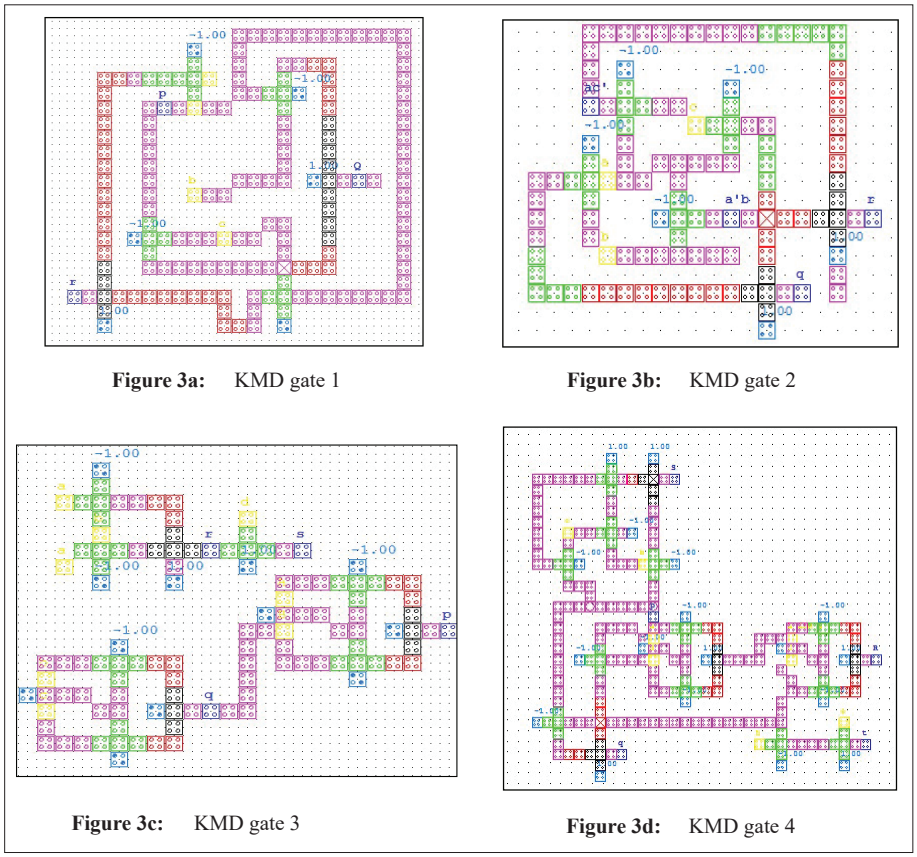


Figure 3a: KMD gate 1

Figure 3b: KMD gate 2

Figure 3c: KMD gate 3

Figure 3d: KMD gate 4

Figure 3: QCA realisation of KMD gates

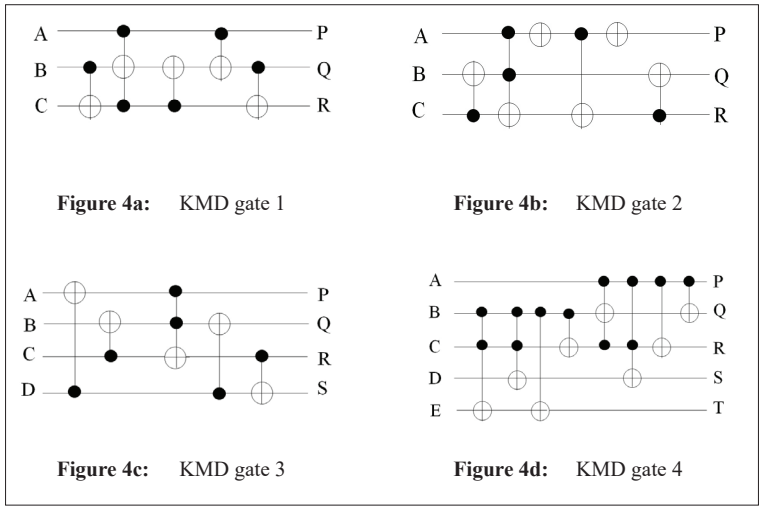


Figure 4a: KMD gate 1

Figure 4b: KMD gate 2

Figure 4c: KMD gate 3

Figure 4d: KMD gate 4

Figure 4: Quantum structure of KMD gates

summed to generate the final result. The basic module of the sutra is 2×2 Vedic multiplier and adder. The repeated arrangement of the 2×2 multiplier would derive the construction of n-bit multiplication. Thus, the computation is very fast as this requires a much less number of steps (Kamaraj *et al*., 2017).

Procedure for Vedic multiplication:

1. The least significant bit of the two numbers is multiplied to form the LSB of the result (vertical).
2. The next higher bits are cross multiplied with each other and the results are added together to produce the next digit of multiplication.
3. The carry part of step 2 is added to the next level sum output to form the next higher bit.
4. All the bits are processed in the same way as in step 2 and step 3 until the last digit of the operand is reached.
5. Record the final product of the Vedic multiplication.

2×2 Vedic multiplier

A two bit multiplication of the two numbers A×B could be carried out in the following manner. The logical expression of the final product is,

$P_0=A_0.B_0$;
$P_1=(A_1.B_0) \oplus (A_0.B_1)$;
$P_2=(A_0.A_1.B_0.B_1) \oplus (A_1.B_1)$;
$P_3=A_0.A_1.B_0.B_1$

It requires 4 AND operations and 2 ADD operations. Graphically, it is represented as in Figure 5.

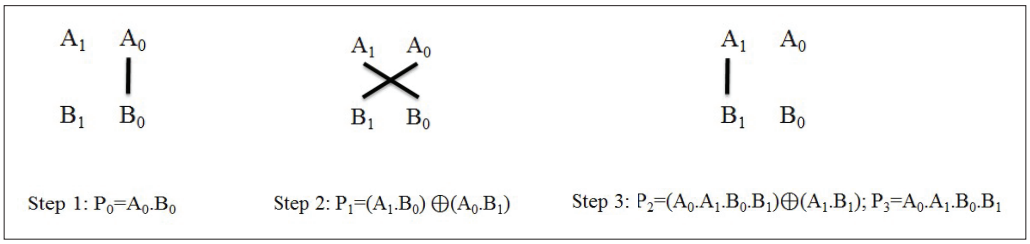


Figure 5: Graphical representation of 2×2 Vedic multiplication steps

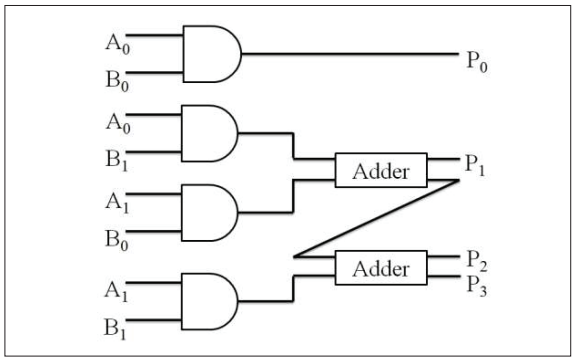


Figure 6a: The hardware architecture of 2-bit Vedic multiplier

The corresponding hardware architecture of the 2×2 Vedic multiplier is depicted in Figure 6a. It has logical AND gates and adders for calculating the product terms. Fault tolerant reversible KMD gates structure of the Vedic multiplier is shown in Figure 6b. In this structure all the functional modules are designed using KMD gates only.

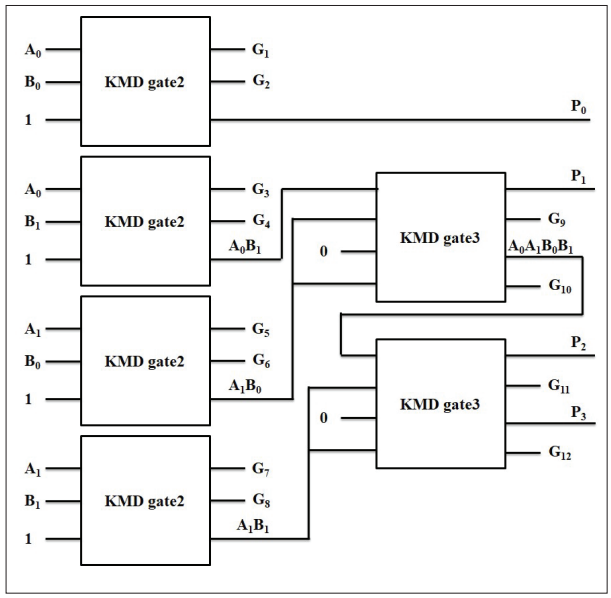


Figure 6b: The reversible logic structure of 2×2 Vedic multiplier using KMD gates

4×4 Vedic multiplier

The 4-bit Vedic multiplier (VM) module is constructed using the 2-bit Vedic multiplier unit (VM_i) four times, three 4-bit ripple carry adders and one half adder gate, which are shown in Figure 7. The inputs A_i ($A_3A_2A_1A_0$) and B_i ($B_3B_2B_1B_0$) are specified to 2-bit Vedic multiplier bitwise, and then the multiplier output is forwarded to the 4-bit RCA adder. The output from the RCA adder consists of 4-bit sum output and a 1-bit carry value. The half adder is used to sum the carry at the first two phases of ripple carry adder. The output of 4-bit multiplier consists of 8-bit product term (P_i - P_7…P_0) (Gowthami & Satyanarayana, 2018).

In a similar way, higher order Vedic multipliers are constructed with the 2-bit VM_i as the base module and RCA adders for summation of the partial products. The n-bit Vedic multiplier uses four n/2-bit multipliers, one n-bit RCA adder, one n-bit full adder, and one [(n/2)−1] bit RCA adder (using only half adder). For example, construction of 16-bit Vedic multipliers by this comprehensive structure requires four 8-bit multiplier units, one 16-bit RCA adder, one 16-bit full adder, and one 7-bit RCA adder (using only half adder). General n-bit Vedic multiplication unit construction using this is illustrated in Figure 8 (Kamaraj *et al*., 2018b).

QCA realisation of reversible Vedic multiplier

The necessary modules for designing a multiplier are AND gate, half adder, and a full adder. These functions could be derived from KMD gates. The reversible Vedic multiplier modules are designed with fault-tolerant reversible gates and it is called fault-tolerant reversible Vedic multiplier.

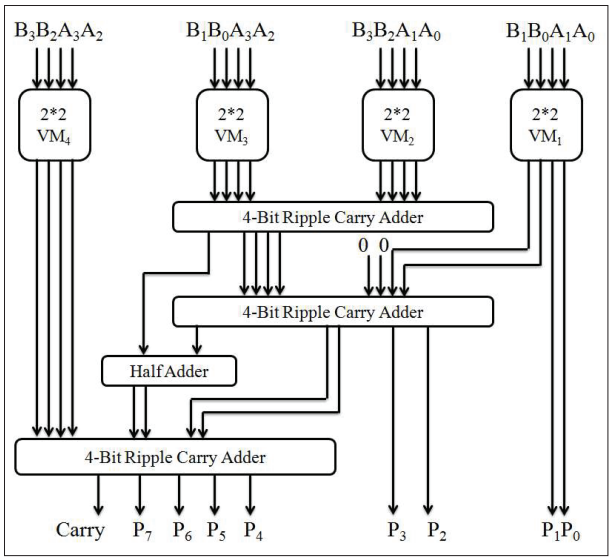


Figure 7: The hardware structure of 4-bit Vedic multiplier

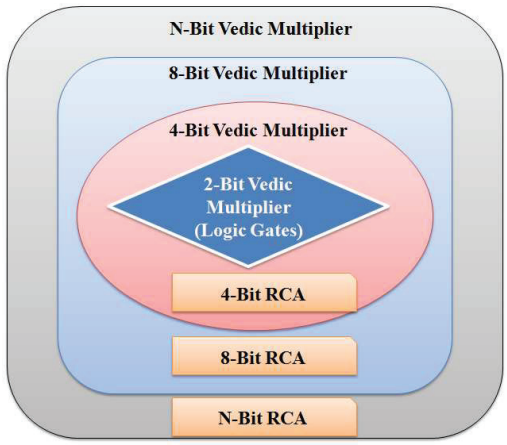


Figure 8: Generalised construction of n-bit Vedic multiplier

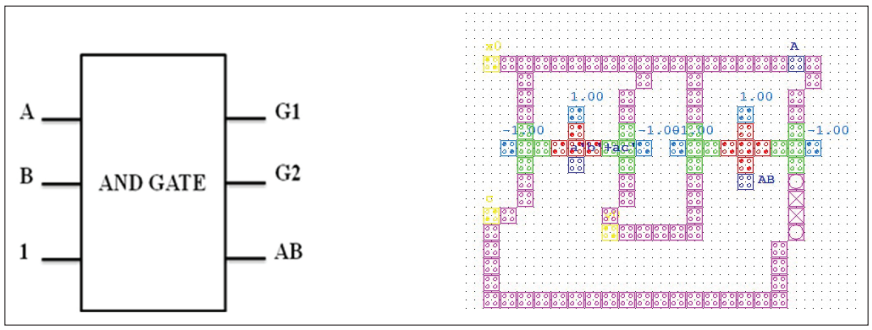


Figure 9: Fault-tolerant reversible AND gate and QCA structure using KMD gate 2

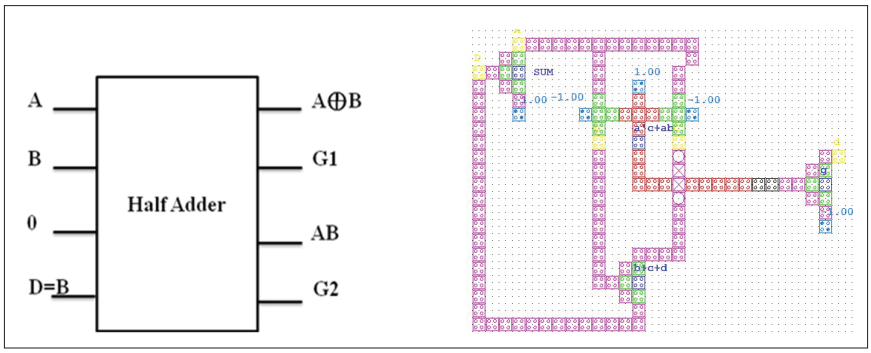


Figure 10: Fault-tolerant reversible half adder and QCA structure using KMD gate

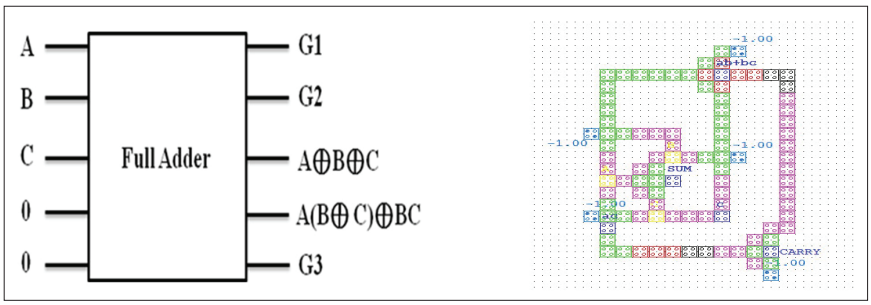


Figure 11: Fault-tolerant reversible full adder and QCA structure using KMD gate 4

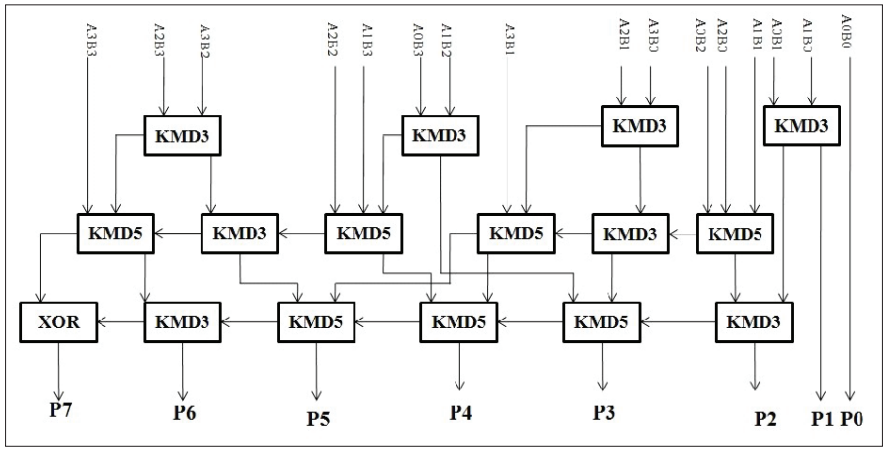


Figure 12: Proposed fault tolerant reversible Vedic multiplier

Fault-tolerant reversible AND gate

By setting logic '1' in the third input of KMD gate 2, AND gate function is derived. The remaining outputs are called garbage outputs (G). In that way, many logical functions can be derived from the single gate. Figure 9 shows the schematic diagram and QCA realisation of AND gate using KMD gate 2.

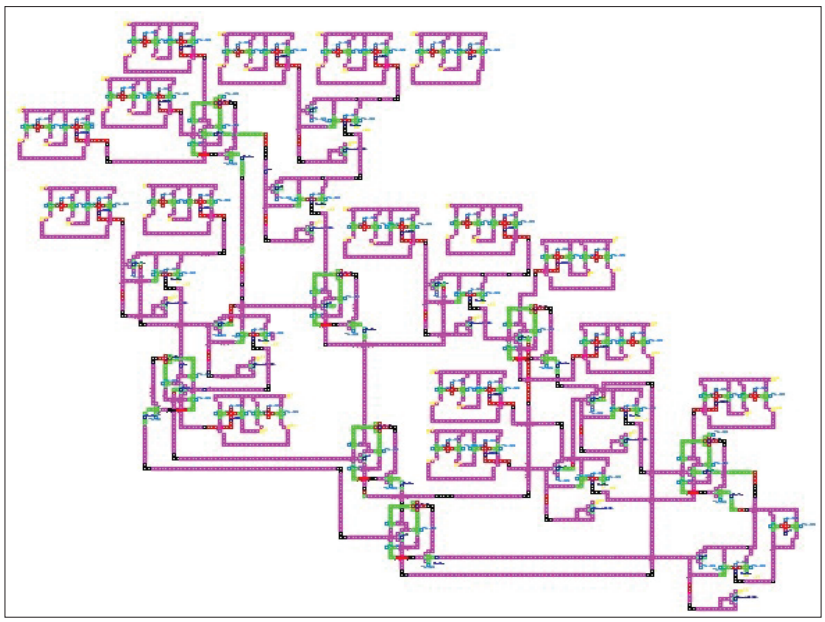


Figure 13: QCA structure of proposed fault tolerant reversible Vedic multiplier

Fault-tolerant reversible half adder

By setting logic '0' in the third input of KMD gate 3 and fourth input as a second input (B), the half adder can be obtained. The remaining outputs are called garbage outputs (G). Figure 10 shows the schematic diagram of half adder using KMD gate 3 and its QCA realisation.

Fault-tolerant reversible full adder

Constant input logic '0' set at fourth and fifth input of KMD gate 4, would make it a full adder. The remaining outputs are called garbage outputs (G). Figure 11 shows the schematic diagram of full adder using KMD gate 4 and its QCA realisation.

Fault-tolerant reversible Vedic multiplier

The fault-tolerant reversible Vedic multiplier is constructed using three KMD gates. In this multiplier, the multiplication process includes only six steps. The addition process is computed by using KMD gates. Here KMD gates 2, 3 and 4 are used to generate the AND function, half adder and full adder, respectively. The fault tolerant reversible Vedic multiplier using KMD gates and its corresponding QCA structure is given in Figures 12 and 13, respectively.

RESULTS AND DISCUSSION

The 4-bit Vedic multiplier depicted in Figure 7 has been constructed using Fault-tolerant reversible KMD gates as shown in Figure 12. The corresponding QCA architecture is designed in QCA designer 2.0.3. Fault-tolerance of the Vedic multiplier has been achieved in two ways: (i) designing it fully with Fault-tolerant KMD gates and (ii) constructing with a combination of fault-tolerant KMD and conventional reversible gates (Fredkin, Toffoli). In both of these approaches, the Vedic multiplier is a fault-tolerant reversible multiplier.

The 2×2 Vedic multiplier has AND gate and half adders as described in the previous section. The total cost for construction in approach 1 is 110. Similarly, the higher order multipliers are constructed from the lower order multipliers. The cost calculation of individual modules of the multiplier and the total costs are listed in Table 3. The total cost includes the sum of quantum cost, garbage output, constant inputs and the number of gates.

In approach 2, the AND gate is constructed using a Fredkin gate instead of KMD gates. However, it is a fault-tolerant reversible multiplier. The cost calculation of individual units and the total costs are shown in Table 4.

Table 3: Performance of fault-tolerant reversible Vedic multiplier (Approach 1)

Functional module	Quantum cost	Garbage output	Constant input	Number of gates (primitive)	Number of gates	Total cost (QC + GO + CI + NoG)	Logical calculations
2-bit fault-tolerant reversible Vedic multiplier							
AND gate	10	2	1	6	1	19	2α+4β+3γ
Half adder	9	2	1	5	1	17	5α+2β+1γ
Full adder	22	3	2	8	1	35	6α+5β+2γ
2-bit VM	58	12	6	34	6	110	18α+20β+14γ
4-bit fault-tolerant reversible Vedic multiplier							
4-bit adder	88	12	8	32	4	140	24α+20β+8γ
4-bit VM	496	84	48	232	36	860	144α+140β+80γ

Table 4: Performance of fault-tolerant reversible Vedic multiplier (Approach 2)

Functional module	Quantum cost	Garbage output	Constant input	Number of gates (primitive)	Number of gates	Total cost (QC + GO + CI + NoG)	Logical calculation
2-bit fault-tolerant reversible Vedic multiplier							
AND gate (Fredkin)	3	2	1	1	1	6	2α+4β+1γ
Half adder	9	2	1	5	1	12	5α+2β+1γ
Full adder	22	3	2	8	1	27	6α+5β+2γ
2-bit VM	30	12	6	14	6	48	18α+20β+8γ
4-bit fault-tolerant reversible Vedic multiplier							
4-bit adder	88	12	8	32	4	108	24α+20β+8γ
4-bit VM	384	84	48	152	36	516	144α+140β+48γ

Table 5: Performance comparison of existing multipliers with proposed multiplier

Performance measures	Conventional multipliers		Vedic multiplier			Proposed Vedic multiplier	
	Valinataj, 2017	Haghparast *et al*., 2009	Saligram & Rakshith, 2013	Rakshith & Saligram, 2013	Gowthami & Satyanarayana, 2018	Approach 1	Approach 2
Quantum cost	177	137	164	162	128	110	48
Garbage output	49	28	43	62	40	12	12
Constant input	49	28	33	29	31	6	6
Number of gates	28	28	33	37	31	14	14
Logical calculations	128α+78β+28γ	71α+36β	-	-	-	18α+20β+14γ	18α+20β+8γ
area (μm^2)	-	-	-	-	-	3.7	3.7

Table 6: Percentage of improvement of the proposed multiplier

Performance measures	% of improvement of the proposed multiplier w.r.t. Conventional multipliers using				Vedic multiplier using					
	ZPLG (Valinataj, 2017)		HNG (Haghparast *et al.*, 2009)		HNG and NFT (Saligram & Rakshith, 2013)		HNG (Rakshith & Saligram, 2013)		BME and HNG (Gowthami & Satyanarayana, 2018)	
	Approach 1	Approach 2	Approach 1	Approach 2	Approach 1	Approach 2	Approach 1	Approach 2	Approach 1	Approach 2
Quantum cost	37.85 %	72.88 %	19.70 %	64.96 %	32.92 %	70.73 %	32.09 %	70.37 %	14.06 %	62.5 %
Garbage output	75.51 %		57.14 %		72.09 %		80.64 %		70 %	
Constant input	87.75 %		78.57 %		81.81 %		79.31 %		80.64 %	
Number of gates	50 %		50 %		57.57 %		62.16 %		54.83 %	

The designed fault-tolerant reversible Vedic multiplier cost performance was compared with the existing conventional and reversible Vedic multipliers and they are shown in Table 5. The performance of the proposed method shows an improvement compared to the existing multipliers in terms of quantum cost, garbage output, constant input, and logical calculations. The percentage of improvement is shown in Table 6 with respect to the existing multitpliers.

CONCLUSION

In general, computation speed of a system is based on the hardware architecture and the data path design. In this paper, an *Urdhwa Triyakbhyam*-based Vedic multiplier has been designed in reversible logic. Vedic multipliers perform computations in minimum number of steps and therefore faster. The necessary functional modules are AND logic, half adder and full adder. These functional modules are constructed in two different approaches. In the first approach all the functional modules are constructed using fault tolerant reversible KMD gates only, and in the second approach combination of Fredkin and KMD gates are used. The functional simulation is performed in QCA environment using QCADesigner 2.0.3. The performance measure shows that the proposed fault-tolerant reversible Vedic multiplier has improved in quantum cost (14 – 72 %), garbage output (57 – 80 %), constant input (78 – 87 %), and a number of gates (50 – 62 %) compared to the existing design. Further, its logical calculation or hardware complexity is $13\alpha+11\beta+6\gamma$, which is comparable with the existing design. Thus, it is concluded that the computation speed and efficiency can be improved by crosswise and vertical multiplication for the proposed fault-tolerant reversible Vedic multiplier.

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